	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	709	method near10 void near1 free	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:20
2	BRS	L2	3004	contact near1 pad$1 near10 bond$3 near1 pad$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:21
3	BRS	L3	28	gap near10 ((chip or component) and substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:23
4	BRS	L5	0	3 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:23
5	BRS	L6	3	4 and pressure	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:23

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L7	3	6 and energy	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:23
7	BRS	L4	4	1 and 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/06 23:25

	U	1	Document ID	Title	Current OR
1	☒	☐	US 6331737 B1	Method of encapsulating thin semiconductor chip-scale packages	257/787
2	☒	☐	US 6107123 A	Methods for providing void-free layers for semiconductor assemblies	438/125
3	☒	☐	US 5834339 A	Methods for providing void-free layers for semiconductor assemblies	438/125
4	☐	☐	US 4366187 A	Immersion curing of encapsulating material	427/96